CALL FOR PAPERS

ISLPED 2023

INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN

http://www.islped.org

TU Wien, Vienna, Austria
August 7–8, 2023

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Organizing Committee and Symposium Officers:

General Co-Chairs
Axel Jantsch, *TU Wien*
axel.jantsch@tuwien.ac.at
Swaroop Ghosh, *Penn State*
szg212@psu.edu

Program Co-Chairs
Umit Ogras, *Wisconsin Univ.*
uogras@wisc.edu
Pascal Meinerzhagen, *Intel*
pascal.a.meinerzhagen@intel.com

Local Arrangements
Thilo Sauter, *TU Wien*
thilo.sauter@tuwien.ac.at
Maximilian Goetzinger, *TU Wien*
maximilian.goetzinger@tuwien.ac.at

Treasurer
Mehdi Kamal, *USC*
mehdi.kamal@usc.edu

Publication Chair
Younghyun Kim, *Wisconsin Univ.*
younghyun.kim@wisc.edu

Web/Registration Chair
Meron Demissie, *UMich*
mdemissi@umich.edu

Publicity Chairs
Semeen Rehman, *TU Wien*
semeen.rehman@tuwien.ac.at
Linghao Song, *UCLA*
linghaosong@cs.ucla.edu
Jae-Joon Kim, Pohang Univ.
kimjaejoon@snu.ac.kr

Design Contest Chair
Rajesh Kedia, *IITH*
rkedia@cse.iith.ac.in
Florian Huemer, *TU Wien*
florian.huemer@tuwien.ac.at

Pending sponsorship by the **ACM Special Interest Group on Design Automation (SIGDA),** the **IEEE Circuits and Systems Society (CASS)** and the **IEEE Council on Electronic Design Automation (CEDA).**

The International Symposium on Low Power Electronics and Design (ISLPED) is the premier forum for presentation of innovative research in all aspects of low power electronics and design, ranging from process technologies and analog/digital circuits, simulation and synthesis tools, AI/ML-enhanced EDA/CAD, system-level design, and optimization, to system software and applications. Specific topics include, but are not limited to, the following three main tracks and sub-areas:

1. Technology, Circuits, and Architecture	**2. EDA, Systems, and Software**
1.1. Technologies Low-power technologies for device, interconnect, logic, memory, 2.5/3D, cooling, harvesting, sensors, optical, printable, biomedical, battery, and alternative energy storage devices and technology enablers for non-Boolean and quantum/quantum-inspired compute models.	**2.1. CAD Tools and Methodologies** CAD tools, methodologies, and AI/ML-based approaches for low-power and thermal-aware design. AI/ML for acceleration of circuit simulation and IP block design convergence. Power estimation, optimization, reliability, and variation impact on power optimization at all levels of design abstraction: physical, circuit, gate, register transfer, behavior, and algorithm.
1.2. Circuits Low-power circuits for logic, memory, reliability, yield, clocking, resiliency, near-/sub-threshold, and assist schemes; Low-power analog/mixed-signal circuits for wireless, RF, MEMS, AD/DA Converters, I/O, PLLs/DLLS, imaging and DC-DC converters; Energy-efficient circuits for emerging applications (e.g., biomedical, in-vitro sensing, autonomous), circuits using emerging technologies; Cryogenic circuits. Design technology co-optimization (DTCO) for low power.	**2.2. Systems and Platforms** Low-power, power-aware, and thermal-aware system design including data centers, SoCs, embedded systems, Internet-of-Things (IoT), wearable computing, body-area networks, wireless sensor networks, and system-level power implications due to reliability and variability. Applications of AI/ML-based solutions and brain-inspired computing to power-aware system and platform design.
1.3. Logic and Architecture Low-power logic and microarchitecture for SoC designs, processor cores (compute, graphics, and other special purpose cores), cache, memory, arithmetic/signal processing, cryptography, variability, asynchronous design, and non-conventional computing. System technology co-optimization (STCO) for low power.	**2.3. Software and Applications** Energy-efficient, energy/thermal-aware software and application design, including scheduling and management, power optimization through HW/SW codesign, and emerging low-power AI/ML applications.
3. Crosscutting Topics	
3.1. AI/ML Hardware Low-power AI/ML HW techniques including approximations, application driven optimizations, in-memory/energy-efficient accelerations, and neuromorphic computing; Energy-efficient AI/ML HW using emerging technologies (including quantum computing).	
3.2. Hardware and System Security Low-power hardware security primitives (PUF, TRNG, cryptographic/post-quantum cryptographic accelerators), nano-electronics security, supply chain security, IoT security and AI/ML security; Energy-efficient approaches to system security.	
4. Industrial Design Track	
ISLPED'23 solicits papers for an "Industrial Design" track to reinforce interaction between the academic research community and industry. Industrial Design track papers have the same submission deadline as regular papers and should focus on similar topics but are expected to provide a complementary perspective to academic research by focusing on challenges, solutions, and lessons learnt while implementing industrial-scale designs.	

Technical Paper Submission Deadlines: Abstract registration by March 6, 2023, at 11:59pm PST
Full paper due by March 13, 2023, at 11:59pm PST

Invited Talk, Panel, and Embedded Tutorial Proposals Deadline: April 10, 2023

Notification of Paper Acceptance: May 22, 2023

Submission of Camera-Ready Papers: June 19, 2023

Submissions (not published/accepted/under review by another journal, conference, symposium, or workshop) should be full-length papers of **up to 6 pages** (PDF format, double-column, US letter size, using the IEEE Conference format, available at (https://www.ieee.org/conferences/publishing/templates.html) including all illustrations, tables, references, and an abstract of no more than 250 words. **Submissions must be anonymous**. Submissions failing above requirements will be automatically rejected. Accepted papers will be submitted to the IEEE Xplore Digital Library and the ACM Digital Library. ISLPED'23 will present three Best Paper Awards based on the ratings of reviewers and a panel of judges.

ISLPED also features a Low Power Design Contest with live demonstrations and awards. Submissions are due on May 15, 2023. More details will soon be available on the conference web page.

There will be several invited talks by industry and academic thought leaders on key issues in low power electronics and design. The Symposium may also include embedded tutorials to provide attendees with the necessary background to follow recent research results, as well as panel discussions on future directions in low power electronics and design. Proposals for invited talks, embedded tutorials, and panels should be sent by email to the ISLPED'23 Technical Program Co-Chairs, Umit Ogras (uogras@wisc.edu) and Pascal Meinerzhagen (pascal.a.meinerzhagen@intel.com) by the deadline listed above.

Participants interested in exhibiting at the Symposium should contact the General Co-Chairs by May 1, 2023.